CSCI 210: Computer Architecture
Lecture 24: Datapath

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Slides from Cynthia Taylor

Announcements

- Problem Set 7 due today

- Lab 6 due Sunday

- Office Hours today 13:30–14:30 pm

Amdahl's Law

$$\text{Execution time after improvement} = \frac{\text{Execution Time Affected}}{\text{Amount of Improvement}} + \text{Execution Time Unaffected}$$

Amdahl’s law example

- A program originally takes 30 seconds to run
- One third of the execution time comes from a single loop
- With some clever programming, you speed the loop up such that it runs twice as fast
- How long does the improved program take to run?

$$\text{Execution time after improvement} = \frac{\text{Execution Time Affected}}{\text{Amount of Improvement}} + \text{Execution Time Unaffected}$$

What was the overall speedup due to the improved loop?

- The original program took 30 s
- The new program took 25 s
- Speedup = Original Time / New Time
- Speedup = 30 s / 25 s = 1.2

Amdahl's Law and Parallelism

Our program is 90% parallelizable (segment of code executable in parallel on multiple processor cores) and runs in 100 seconds with a single core. What is the execution time if you use 4 cores (assume no overhead for parallelization)?

	Execution Time
A	25 seconds
B	32.5 seconds
C	50 seconds
D	92.5 seconds
E	None of the above

$$\text{Execution time after improvement} = \frac{\text{Execution Time Affected}}{\text{Amount of Improvement}} + \text{Execution Time Unaffected}$$

Amdahl’s Law

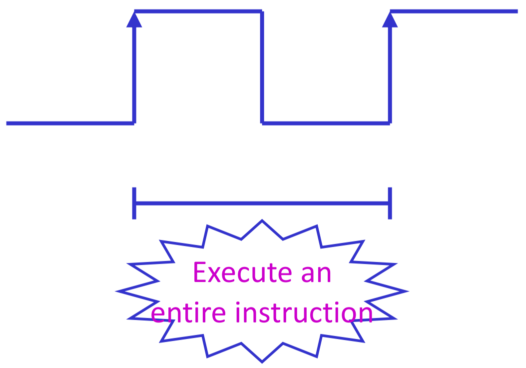
So what does Amdalh’s Law ***mean*** at a high level?

Selection	“BEST” message from Amdahl’s Law
A	Parallel programming is critical for improving performance
B	Improving serial code execution is ultimately the most important goal.
C	Performance is strictly tied to the ability to determine which percentage of code is parallelizable.
D	The impact of a performance improvement is limited by the percent of execution time affected by the improvement
E	None of the above

Performance Questions?

The Big Picture: The Performance Perspective

- Processor design (datapath and control) will determine:
  - Clock cycle time
  - Clock cycles per instruction
- Starting today:
  - Single cycle processor:
    - Advantage: One clock cycle per instruction
    - Disadvantage: long cycle time
- ET = Insts * CPI * Cycle Time



The Processor: Datapath & Control

- We're ready to look at an implementation of MIPS simplified to contain only:
  - memory-reference instructions: `lw, sw`
  - arithmetic-logical instructions: `add, sub, and, or, slt`
  - control flow instructions: `beq`

Generic implementation

- Fetch
  - Use the program counter (PC) to supply instruction address
  - Get the instruction from memory
  - Update the program counter to the next instruction
- Decode instruction
  - Read registers
  - Use the instruction to decide exactly what to do
- Execute
  - Perform necessary data manipulation
  - Write to registers

To fetch an instruction, what hardware do we need?

- Fetch
  - Use the program counter (PC) to supply instruction address
  - Get the instruction from memory
  - Update the program counter to the next instruction

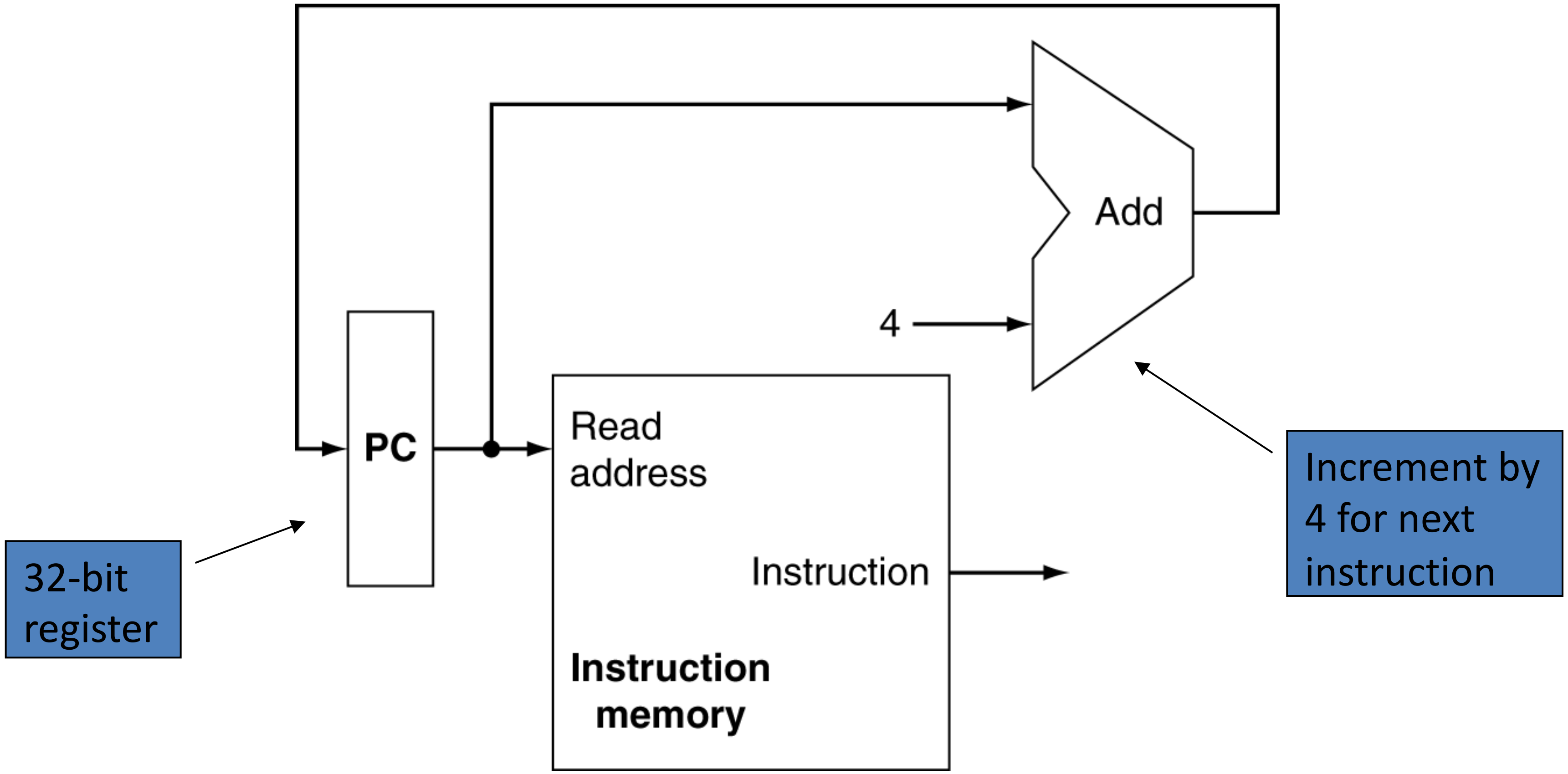
A. Register(s), Memory

B. Register(s), Adder, Memory

C. Register(s), ALU, Memory

D. More than this

Instruction Fetch



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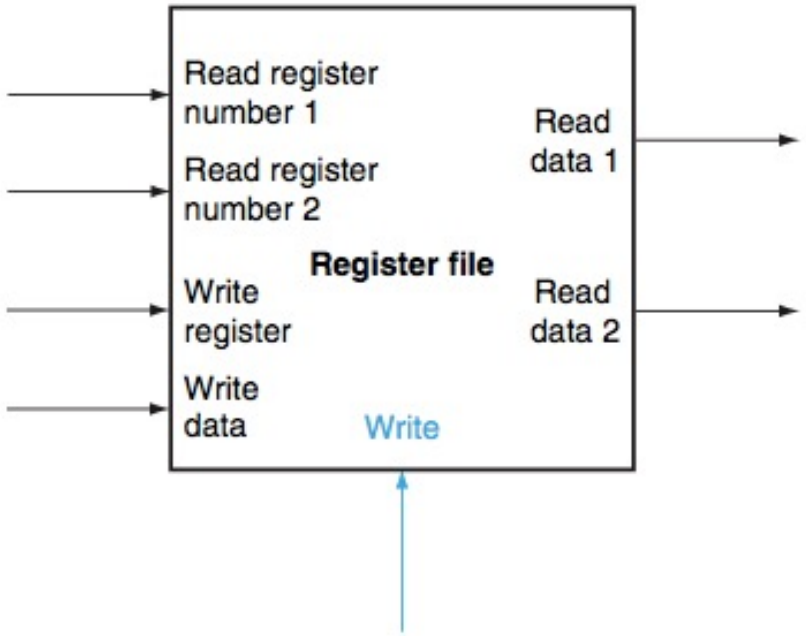
Which of these describes the interface for our register file?

Think about what we will read in and out in different instructions i.e.,
`add $t0, $t0, $t1` vs.
`sw $t0, 16($s3)`

A. Two 32-bit data outputs, three 5-bit select inputs, 1-bit control input
B. Two 32-bit data outputs, three 32-bit select inputs, 1-bit control input
C. Two 32-bit data outputs, three 5-bit select inputs, 1 32-bit data input, 1-bit control input
D. Two 32-bit data outputs, 2 32-bit select inputs, 1 5-bit data input, 1-bit control input
E. None of the above

Register File



Reading

- Next lecture: Control Path
  – Section 5.3